

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Atty. Docket: 02-GR1-123  
Nicolas CARRIERE et al. : Applications Branch  
Serial No. (Not Yet Assigned) :  
Filed: HEREWITH :  
For: *PROCESS FOR FABRICATING A TRANSISTOR WITH  
A METAL GATE, AND CORRESPONDING TRANSISTOR*

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

SIR:

The attached Form PTO-1449 provides a listing of information which may be relevant to the subject application. This IDS is not intended as a representation that better art is not available, nor that other art than that identified exists; nor that the information provided is prior art; nor that a search has been made.

This IDS is submitted under:

- ☒ 37 CFR 1.97(b) - No Fee.  
☐ 37 CFR 1.97(c) - No Fee, with Certification.  
☐ 37 CFR 1.97(c) - Fee.  
☐ 37 CFR 1.97(d) - Fee, Certification & Petition.

The Commissioner is authorized to charge any required fees under 37 CFR 1.17(p) and (i) (1) to Deposit Account No. 50-1556.

Respectfully submitted,

Date: 3/25/04

By: Jose Gutman

Jose Gutman  
Registration No. 35,171

FLEIT, KAIN, GIBBONS, GUTMAN, BONGINI & BIANCO P.L.  
551 NW 77th Street  
Suite 111  
Boca Raton, Florida 33487  
Telephone: (561) 989-9811  
Facsimile : (561) 989-9812

Form PTO-1449	U.S. Dept. of Commerce Patent & Trademark Office	Atty. Docket: 02-GR1-123	Serial No. Not Yet Assigned
<b>List of Documents Cited by Applicant</b> (Use several sheets if necessary)		Applicant: Nicolas CARRIERE et al.	
		Filing Date: HEREWITH	

### U.S. PATENT DOCUMENTS

Ex'rs In'i	Document Number	Date	Name	Class	Sub- class	Filing Date, if applicable
	AA1	5,352,631	October 4, 1994	Sitaram et al.		
	AA2	6,153,485	November 28, 2000	Pey et al.		
	AA3	6,228,722	May 8, 2001	Lu		
	AA4	6,297,135	October 2, 2001	Talwar et al.		

### FOREIGN PATENT DOCUMENTS

Document Number	Date	Country	Class	Sub- class	Trans'l'n Yes/No

### OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AA5	Tavel, B. et al., "Totally Silicided (COSI2) Polysilicon: a novel approach to very low-resistive gate (20MEGA/ ) without metal CMP nor etching", International Electron Devices Meeting 2001, IEDM. Technical Digest, IEEE, December 2, 2001, pp. 825-828, XP001075639.
	AA6	French Preliminary Search Report dated November 25, 2003 for French Application No. 03 03647.

Examiner:	Date Considered:
-----------	------------------

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.